



SHRI VITHAL EDUCATION & RESEARCH INSTITUTE'S
COLLEGE OF ENGINEERING, PANDHARPUR

Gopalpur -Ranjani Road, Gopalpur, P.B. No. 54, Tal - Pandharpur- 413 304,

Dist. Solapur (Maharashtra) Ph.: (02186) 225083, Fax: (02186) 225082.

(Approved by AICTE, New Delhi and affiliated to Solapur University, Solapur)

FDP Report

- **Name of FDP:** VLSI Design using Open Source Methodologies and challenges in Digital Integrated Circuits and Memory Design
- **Date:** 09th Dec. to 13th Dec. 2019
- **No. of Participants:** 42
- **Brief report:** Department of CSE has organized five days faculty development program on “VLSI Design using Open Source Methodologies and challenges in Digital Integrated Circuits and Memory Design”, from 09th Dec. to 13th Dec. 2019. The FDP was sponsored by IIIT DM, Jabalpur. For this FDP, total 42 faculties were participated from different institutes. Dr. Gaurav Trivedi (IIT Guwahati), Prof. Vineet Sahula (MNIT Jaipur), Dip Prakash Samajdar (IIITDM Jabalpur) and Dr. Menka Yadav (MNIT Jaipur) were resource person. This FDP was conducted in collaboration with IIITDM, Jabalpur. E&ICT Academy and funded by Ministry of Electronics and IT, Government of India.

Photographs of FDP

Patrons

Dr. B. P. Ronge
PRINCIPAL, College of Engineering, Pandharpur.

Convener

Dr. P. M. Pawar
DEAN ACADEMICS and HOD CIVIL Department,
College of Engineering, Pandharpur

Coordinator

Dr. Bhuvaneshwari C. Melinmath
HOD, CSE Department,
College of Engineering, Pandharpur

Dr. A. S. Vibhute

HOD, E&TC Department,
College of Engineering, Pandharpur

Co-Coordinator

Mr. S. P. Swami
Asst. Professor,
E&TC, College of Engineering, Pandharpur

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MAJOR TOPICS

- Brief introduction RISC-V ISA
- Overview of RISC-V based micro-processor and its related SoC
- Overview of QFN48 package, pads, macros and memory in MAGIC
- Idea of chip-planning, aspect ratio, utilization factor, power planning, decoupling capacitor, pads/memory and macro placement
- Introduction to lab to create floorplan for small design
- System-on-Chip (SoC) planning and design concepts overview, Physical design overview
- Standard cells library overview
- Art of layout – Stick diagram + Euler's path using MAGIC
- Characterization of important parameters using ngSPICE
- Introduction to 16-Mask CMOS process and its significance to chip design flow
- Logic synthesis and high fanout net synthesis interactive tutorial using Yosys open source synthesis tool
- Introduction to static timing analysis and the related industry standard reporting formats
- Pre-layout timing analysis of a design using open source STA tool, which includes setup timing analysis for reg2reg and IO
- Introduction to clock tree synthesis (CTS) and its related checks viz. skew, latency, pulse-width, duty cycle
- Placement/Routing/CTS of a design using qflow open source RTL2GDS tool, Perform CTS quality and routing quality checks.
- Post-layout timing analysis using OpenSTA and engineering change order (ECO) using Tritonizer, Full chip integration using MAGIC.

CONTACT US

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**One Week
Faculty Development Program
On
VLSI Chip Design Hands on using
Open Source EDA**

Organized by CSE & E&TC Department,
SVERI's College of Engineering, Pandharpur

Sponsored By
IIITDM, Jabalpur, E&ICT Academy
16th - 20th December 2019

An Initiative of
Ministry of Electronics and IT,
Government of India.



Registration Link:
<http://fdp.sveri.ac.in>



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Sample Attendance

Participant List
 College Name SVERI's College Of Engg. Pandharpur
 FDP Name with Date VLSI Chip Design Hands On using Open source EDA
 16/12/2019 to 20/12/2019

SNo	Name	Faculty/Student/Others	Male/Female	Category(SC/ST/OBC/UR)	Institution
1	Dr. A.S.Vibhute	Faculty	Male	Open (UR)	COE, Pandharpur
2	Dr.S.R.Patil	Faculty	Male	Open (UR)	COE, Pandharpur
3	Dr.M.M.Pawar	Faculty	Female	Open (UR)	COE, Pandharpur
4	Mr. J.S.Hallur	Faculty	Male	Open (UR)	COE, Pandharpur
5	Mr.S.S.Bidwai	Faculty	Male	Open (UR)	COE, Pandharpur
6	Ms.N.P.Kulkarni	Faculty	Female	Open (UR)	COE, Pandharpur
7	Mr.M.S.Mathpati	Faculty	Male	Open (UR)	COE, Pandharpur
8	Mr.D.A.Kumbhar	Faculty	Male	OBC	COE, Pandharpur
9	Ms.G.G.Uhale	Faculty	Female	Open (UR)	COE, Pandharpur
10	Mr.S.A.Inamdar	Faculty	Male	Open (UR)	COE, Pandharpur
11	Mr.A.A.Jadhav	Faculty	Male	Open (UR)	COE, Pandharpur
12	Mr.M.A.Deshmukh	Faculty	Male	OBC	COE, Pandharpur
13	Ms.S.V.Jagtap	Faculty	Female	Open (UR)	COE, Pandharpur
14	Ms.M.Biswas	Faculty	Female	Open (UR)	COE, Pandharpur
15	Ms.S.S.Kadam	Faculty	Female	Open (UR)	COE, Pandharpur
16	Ms.S.Atole	Faculty	Female	OBC	COE, Pandharpur
17	Ms.N.S.Patil	Faculty	Female	Open (UR)	COE, Pandharpur
18	Mr.S.P.Swami	Faculty	Male	OBC	COE, Pandharpur
19	Mr.V.S.Bhong	Faculty	Male	Open (UR)	COE, Pandharpur
20	Mr.N.S.Admile	Faculty	Male	OBC	COE, Pandharpur
21	Mr.A.D.Mali	Faculty	Male	Open (UR)	COE, Pandharpur
22	Mr.D.P.Narsale	Faculty	Male	Open (UR)	COE, Pandharpur
23	Mr.A.M.Kasture	Faculty	Male	Open (UR)	COE, Pandharpur
24	Mr.A.B.Chounde	Faculty	Male	Open (UR)	COE, Pandharpur
25	Ms P B Kashid	Faculty	Female	OBC	COE, Pandharpur
26	Mr.A.A.Jadhav	Faculty	Male	Open (UR)	COE, Pandharpur
27	Ms S.R.Jadhav	Faculty	Female	Open (UR)	COE, Pandharpur
28	Ms. R. M. Shinde	Faculty	Female	Open (UR)	COE, Pandharpur
29	Mr. P.G. Gaikwad	Faculty	Male	Open (UR)	COE, Pandharpur
30	Mr. P.K. Kurzekar	Faculty	Male	OBC	COE, Pandharpur
31	Ms S.S.Bhosale	Faculty	Female	Open (UR)	COE, Pandharpur
32	Mr.R.D.Kulkarni	Faculty	Male	Open (UR)	COE, Pandharpur
33	Mr.H.M.Tamboli	Faculty	Male	OBC	COE, Pandharpur
34	Mr.S.A.Dhanave	Faculty	Male	Open (UR)	COE, Pandharpur
35	Mr.P.K.Magdum	Faculty	Male	Open (UR)	COE, Pandharpur
36	Mr.M.S.Yadrami	Faculty	Male	Open (UR)	COE, Pandharpur
37	Mr.S.C.Ukirde	Faculty	Male	Open (UR)	COE, Pandharpur
38	Ms.S.S.Yadav	Faculty	Female	Open (UR)	COE(POLY), Pandharpur
39	Ms P.B.Maske	Faculty	Female	Open (UR)	COE(POLY), Pandharpur
40	Ms. E. I. Chouhan	Student	Female	Open (UR)	COE, Pandharpur
41	Ms. S. B. Korke	Student	Female	Open (UR)	COE, Pandharpur
42	Ms. A. S. Jadhav	Student	Female	Open (UR)	COE, Pandharpur

B. Q. ...
 HOD,
 Department of Computer Science & Engg.
 SVERI & COE, Pandharpur



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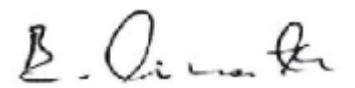
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Sample Certificate




Dr. B. C. Melinamath
HOD CSE